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Sun 501-1102 Memory Board

Configuration Procedures

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Credits and Trademarks

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General Description

The Sun 501-1102 Memory Board provides main memory for the 501-1206 (or 501-1100) CPU board. The 501-1206 CPU board has on-board cache and video memory only.

Each board contains 8 Mbytes of ECC memory and uses the high-speed 64-bit data/address bus on the 501-1206 board for communication with the CPU.

Address Configuration

There are no dip switches on the board; a block of jumper pins on the edge of the board designates the board's base address. Each pair of pins represents 8-Megabtyes of memory installed in the system. When the board is installed vertically in the cardcage, the top jumper pair, labeled "3", represents the fourth memory board, and the bottom pair, labeled "0", represents the first board.

Install ONLY one jumper per board in the position that represents the board number, which is determined by the slot the board occupies. Refer to *Cardcage Slot Assignments and Backplane Configuration Procedures*, Sun PN 813-2004 for tables that define memory board numbering and slot assignment.

When more than one memory board is installed in a system, each board must have unique address configuration; each board must have a jumper setting that is different from any other memory board in the system.

The address jumper pins are accessible from the rear of the system, without removing the board (refer to Figure 1 on the following page).

Terminating Resistor Network

The first memory board installed MUST be placed in Slot 6, and MUST have a terminating resistor network (Sun PN 120-1613) in location 34F on the board. A terminating resistor network should be installed ONLY on the memory board in slot 6.

If additional 501-1102 Memory Boards are installed in slots 2, 3 or 4, you MUST REMOVE the terminating resistor network from the DIP socket at location 34F.

The resistor network terminates key control signals on the "P2" Physical Address Bus to ensure reliable CPU/Memory communication. The illustration that follows shows the location of the socket for the network.

Figure 1 *501-1102 Board Layout*

This illustration supports all revisions of the 501-1102 Memory Board.

Install ONLY ONE jumper in a different position for each board, as shown below. To remove the jumper, use needle-nosed pliers that have a fine point.

Address Select Jumper Block

0 - - - 0 3 IN for 4th Memory Board

0 - - - 0 2 IN for 3rd Memory Board

0 - - - 0 1 IN for 2nd Memory Board

0 - - - 0 0 IN for 1st Memory Board

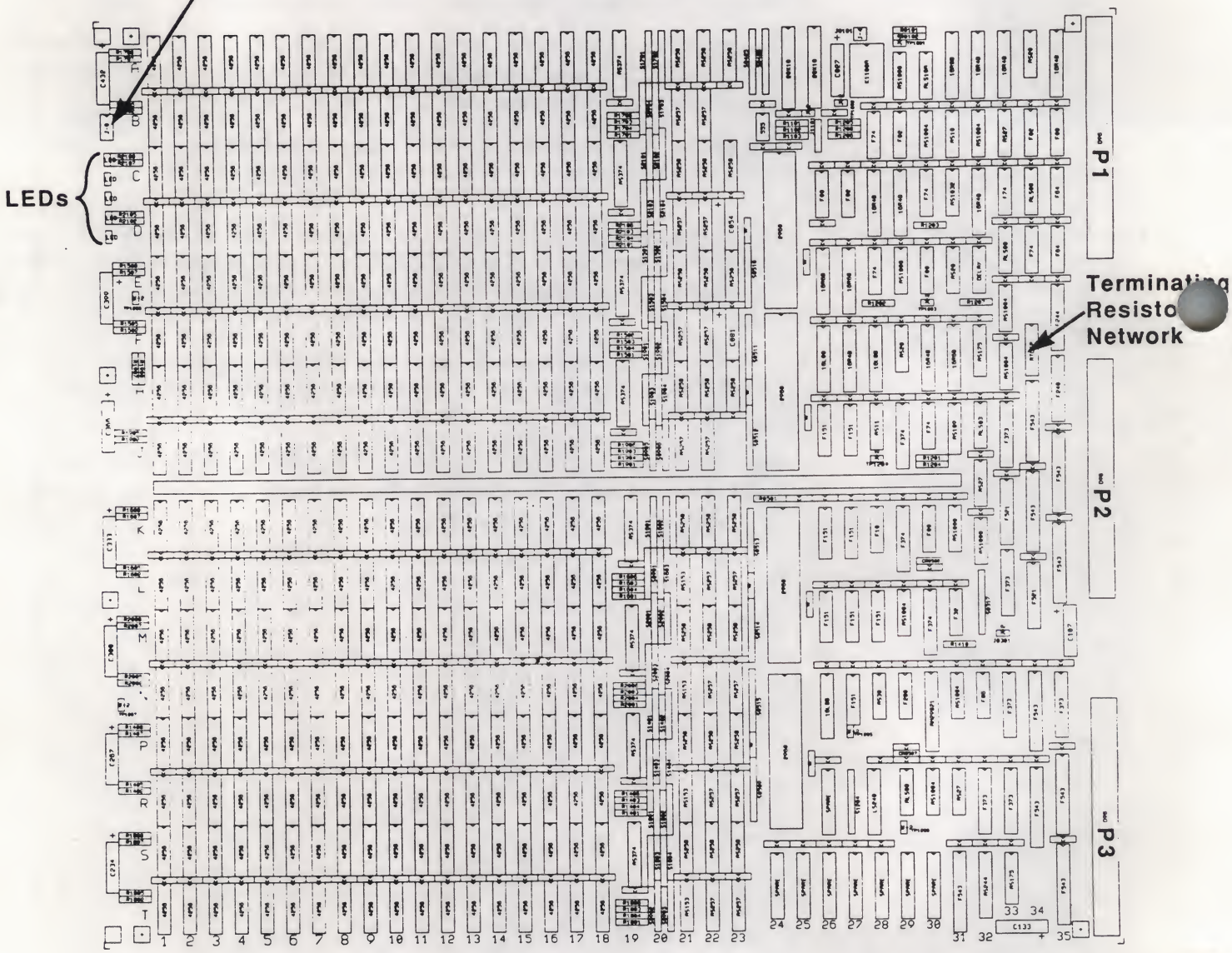

Table 1 *Revision History*

Revision	Date	Comments
Review Draft	15 July 1986	First Draft of this Configuration Procedure.
02-50	21 July 1986	Engineering release of this Configuration Procedure.
05-A	10 October 1986	Production release of this Configuration Procedure.